ABSTRACT OF THE DISCLOSURE

[0050] Embodiments of the present invention include an integrated circuit that has eight queues to receive commands for a memory device, the memory device having four banks, the eight configurable queues having a first queue and a second queue to map to a first bank. The integrated circuit also includes logic to determine the last type of command de-queued, determine a bank designated to receive the next command to be de-queued, inspect the first and the second queues for a type of command matching the last type of command de-queued, de-queue the command that matches the last type of command de-queued, and send the de-queued command to the designated bank. In one embodiment, the designated bank is the next sequential bank after a bank to receive a last de-queued command.